DECEMBER 1976
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Pulsed Power Supply Operation of Selected MM2102 Static RAM

introduction

Static RAMs have a significant number of advantages over dynamic devices, including ease of use and no requirement for refresh. One disadvantage of static RAMs is that they dissipate more power on a per bit basis than dynamic RAMs. This application note will describe a technique by which selected MM2102 Static RAMs can be operated in a standby mode with a very low average power drain.

The SM61480 is an MM2102 that has been selected to ensure operation in the pulsed power mode.

theory of operation

The MM2102 is manufactured using N-channel enhancement mode technology which is key to operation in a pulsed V_{CC} mode. An enhancement mode device conducts current when the gate is a threshold voltage (approximately 1 volt) above that of the source. Once the voltage between the gate and the source is less than the threshold voltage the device is cut off and no current conduction can take place. This characteristic allows data stored in the memory cell to be maintained for short periods of time with the power supply off.

To better understand how data is maintained, consider the MM2102 memory cell (figure 1). Assume the device has been operating in the normal mode (V_{CC} applied) and that node 1 is high and node 2 is low. Capacitor C_4 will be charged to a value near V_{CC} and capacitor C_3 will be charged to a value near ground.

When V_{CC} falls, two things happen in the storage cell:

1. Q_1 starts turning off as V_{CC} (and the gate) begin to fall.
2. Q_2 will turn off when V_{CC} falls below its threshold.

With Q_1 and Q_2 off, the cell is now in a stable condition and will remain stable until the leakage currents discharge C_4 below the trip point of the flip-flop. The charge on the capacitor can be maintained above the trip point by replenishing C_4 on a periodic basis. The replenishing during power-up brings node 1 back to its initial condition each time. The pulsed power mode can be continued indefinitely, resulting in a very iow average power drain.

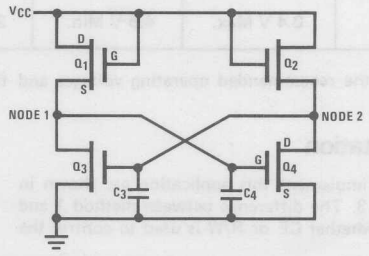


FIGURE 1. MM2102 Memory Cell

DA-B20M126/Printed in U.S.A.

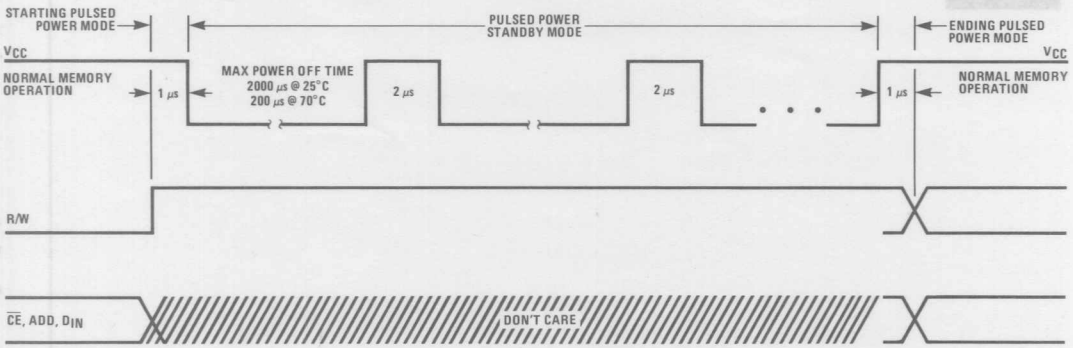


FIGURE 2. Method 1

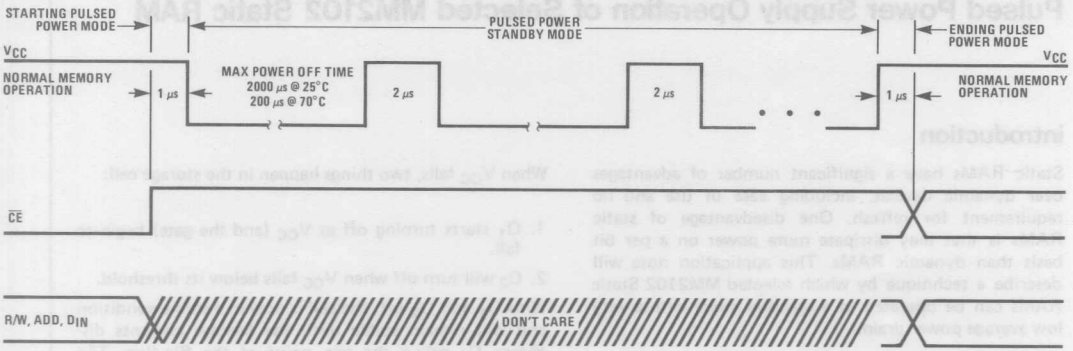


FIGURE 3. Method 2

	V_{CC} Low	V_{CC} High	T_{ON}	T_{OFF}	CE	R/W
Scheme 1	0.4 V Max.	4.5 V Min.	2 μs	2000 μs at 25°C 200 μs at 70°C	Don't Care	2.4 V Min.
Scheme 2	0.4 V Max.	4.5 V Min.	2 μs	2000 μs at 25°C 200 μs at 70°C	2.4 V Min	Don't Care

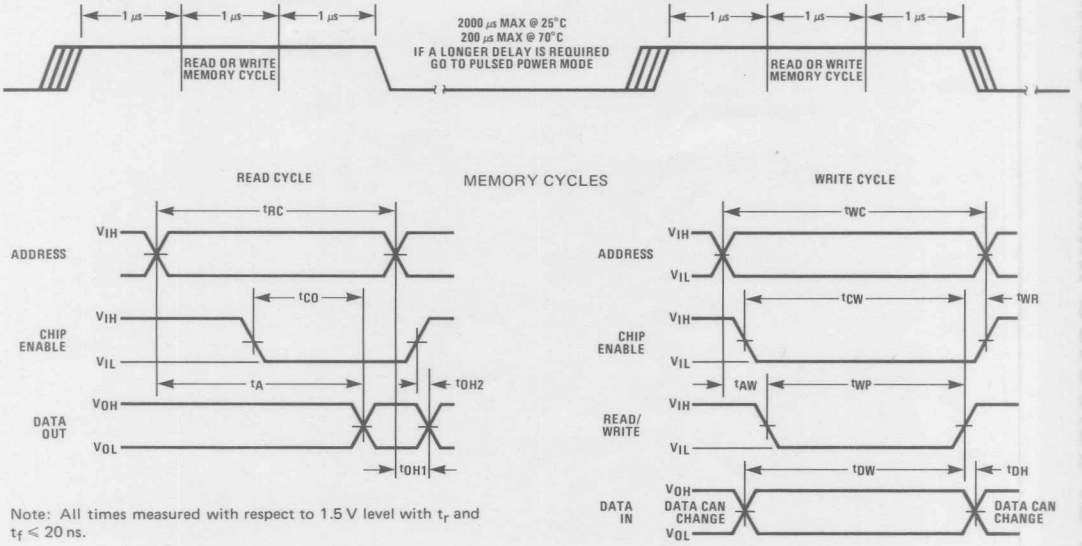
Table I gives the recommended operating voltages and timings for the two different schemes.

implementation

Two ways to implement this application are shown in figures 2 and 3. The difference between method 1 and method 2 is whether $\overline{CE}$ or R/W is used to control the memory.

R/W method 1, or $\overline{CE}$ method 2, should be brought to the 2.4 volt level at least 1 μs prior to the start of the pulsed operation. Once the pulsed mode has ended and the V_{CC} supply has been brought back to its guaranteed operating range, a hold time of at least 1 μs is required before memory operation is attempted. See table I.

Figure 4 illustrates the timing required for powering the memory up for a memory cycle then powering the memory down until the next memory cycle is required or the maximum allowed time for power down is reached. If the next memory cycle is not required within the maximum time allowed for power-down, power-up pulses can be used — this is a combination of the techniques illustrated in figures 2 or 3 and figure 4.



Note: All times measured with respect to 1.5 V level with t_r and $t_f \leq 20$ ns.

FIGURE 4.

Figure 5 illustrates a pulse power circuit suitable for operating an enhancement mode MM2102 RAM. The pulse input can come from any TTL output that can sink at least 2 mA. If the pulse input is driven with a CMOS output, R_2 is not necessary as the V_{OH} of a CMOS part will turn the pass transistor (2N3467) off without a pullup resistor. A 74C902 is a CMOS device that is a good driver for this application.

Figures 6 and 7 show typical characteristics for t_{off} vs temperature and I_{CCAVE} vs duty cycle.

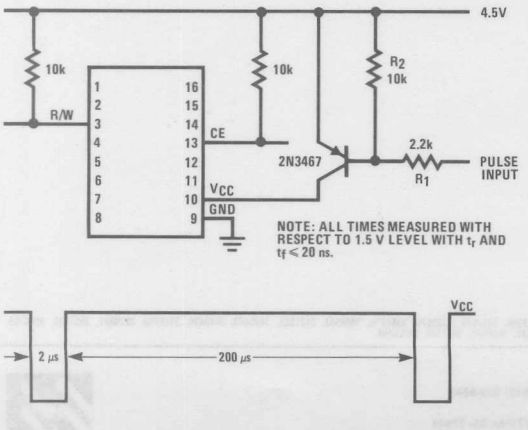


FIGURE 5. Pulse Power Circuit

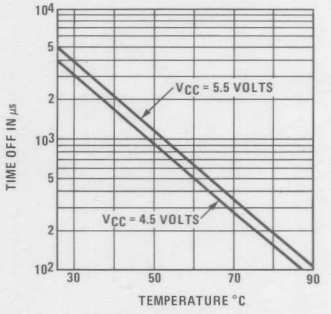


FIGURE 6. T_{OFF} vs Temperature

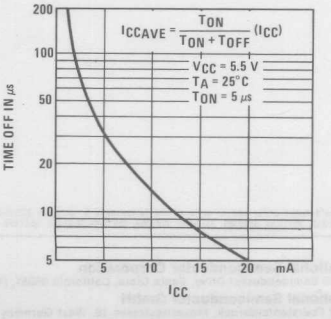
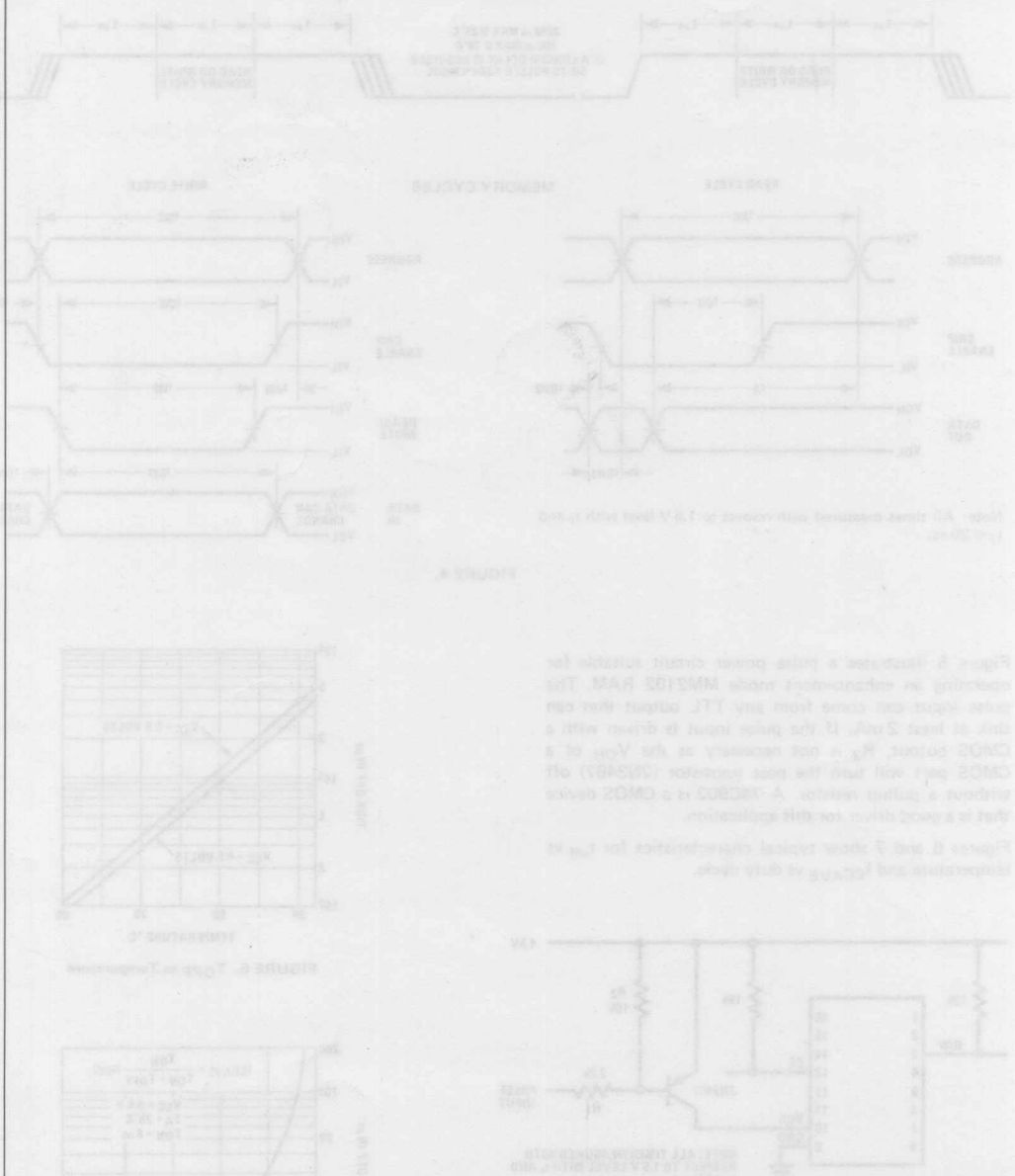


FIGURE 7. I_{CCAVE} vs T_{OFF}

pulsed power supply operation of selected MM2102 static RAM



Manufactured under one or more of the following U.S. patents: 3083262, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571630, 3575609, 3579059, 3593069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3693248.

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AN-172